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### 1 Estimation of hydrodynamic coefficients of a test-bed AUV-SNUUV I by motion test

Kihun Kim; Joonyong Kim; Hang S. Choi; Kyu-Yeul Lee; Woojae Seong;

Oceans '02 MTS/IEEE, Volume: 1, Oct. 29-31, 2002

Page(s): 186 -190

[Abstract] [PDF Full-Text (326 KB)] IEEE CNF

# Tracking down software bugs using automatic anomaly detection

(Hangal, S.) Lam, M.S.;

Software Engineering, 2002. ICSE 2002. Proceedings of the 24rd International Conference on , 19-25 May

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[Abstract] [PDF Full-Text (1285 KB)] IEEE CNF

# 3 Performance analysis and validation of the picoJava processor

Hangal, S.; O'Connor, M.;

Micro, IEEE, Volume: 19 Issue: 3, May-June 1999

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[Abstract] [PDF Full-Text (1024 KB)] IEEE JNL

## 4 Decimation filter compiler for oversampling A/D applications

Hang, S.-S.; Jain, R.;

Acoustics, Speech, and Signal Processing, 1992. ICASSP-92., 1992 IEEE International Conference on ,

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Tsang, J.C.; McKitterick, J.B.; Zolnier, J.A.; O'Connor, J.M.;

High Temperature Electronics Conference, 1998. HITEC. 1998 Fourth International , 14-18 June 1998

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# 2 225 C high temperature silicon-on-insulator (SOI) ASICs for harsh environments

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#### 4 VIS speeds new media processing

Tremblay, M.; O'Connor, J.M.; Narayanan, V.; Liang He;

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# 5 UltraSparc I: a four-issue processor supporting multimedia

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# 7 A 1.45-W/mm, 30-GHz InP-channel power HEMT

Aina, O.; Burgess, M.; Mattingly, M.; Meerschaert, A.; O'Connor, J.M.; Tong, M.; Ketterson, A.; Adesida, I.; Electron Device Letters, IEEE, Volume: 13 Issue: 5, May 1992
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# 9 Growth of high purity InP and fabrication of high sensitivity InP/GaInAs heterojunction phototransistors on silicon by OMVPE

Aina, L.; Mattingly, M.; Burgess, M.; O'Connor, J.M.; Shastry, S.K.; Hill, D.S.; Salerno, J.P.; Davis, A.; Lorenzo, J.P.;

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Aina, L.; Burgess, M.; Mattingly, M.; O'Connor, J.M.; Meerschaert, A.; Tong, M.; Ketterson, A.; Adesida, I.; Electron Device Letters, IEEE, Volume: 12 Issue: 9, Sept. 1991
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# 11 High voltage DMOS power FETs on thin SOI substrates

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Belen Abril Garcia, A.; Gobert, J.; Dombek, T.; Mehrez, H.; Petrot, F.;

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Wong, S.; Cotofana, S.; Vassiliadis, S.;

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## 3 Hybridizing and coalescing load value predictors

Burtscher, M.; Zorn, B.G.;

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Burtscher, M.; Zorn, B.G.;

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# 6 An integrated functional performance simulator

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8 An approach for quantitative analysis of application-specific dataflow architectures

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# 1 Exploring the cache design space for web servers

Parallel and Distributed Processing Symposium., Proceedings 15th International, 23-27 April 2001 Page(s): 8 pp.

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Menasce, D.A.; Gomaa, H.;

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2 Environment for PowerPC microarchitecture exploration

Moudgill, M.; Wellman, J.-D.; Moreno, J.H.;

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Reilly, M.; Edmondson, J.;

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### 5 PAT: state machine based approach to performance modeling for PowerPCTM microprocessors

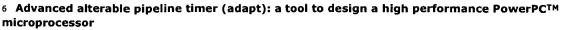
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# 10 Timing analysis for synthesis of hardware interface controllers using timed signal transition graphs

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12 The PowerPC 603 microprocessor: performance analysis and design trade-offs

Poursepanj, A.; Ogden, D.; Burgess, B.; Gary, S.; Dietz, C.; Lee, D.; Surya, S.; Peters, M.; Compcon Spring '94, Digest of Papers. , 28 Feb.-4 March 1994 Page(s): 316 -323

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13 A microarchitectural performance evaluation of a 3.2 Gbyte/s microprocessor bus Stanley, T.; Upton, M.; Sherhart, P.; Mudge, T.; Brown, R.; Microarchitecture, 1993. Proceedings of the 26th Annual International Symposium on , 1-3 Dec. 1993 Page(s): 31 -40

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